## Timer IC circuit separates rep rate and duty cycle control

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Combining both halves of a 556 dual timer with an operational amplifier in this simple circuit enables independent control of the output frequency and the duty cycle. The frequency is adjustable throughout the normal 10-hertz-to-10-kilohertz range of the 556, and the duty cycle is selectable from 1% to 99% of the total waveform period.

As shown in the figure, one half of the 556  $(A_1)$  is connected as an astable multivibrator, oscillating at a frequency given by  $f = 1.4/(R_1 + R_2)C$ . This oscillator is the frequency-governing element in the circuit.

The negative-going edge of signal  $v_1$  periodically triggers timer  $A_2$ , which operates as a monostable multivibrator. An exponential ramp emanating from the threshold port of  $A_1$  drives  $A_2$  through the 531 op amp.

The duty cycle in this timer is determined not by

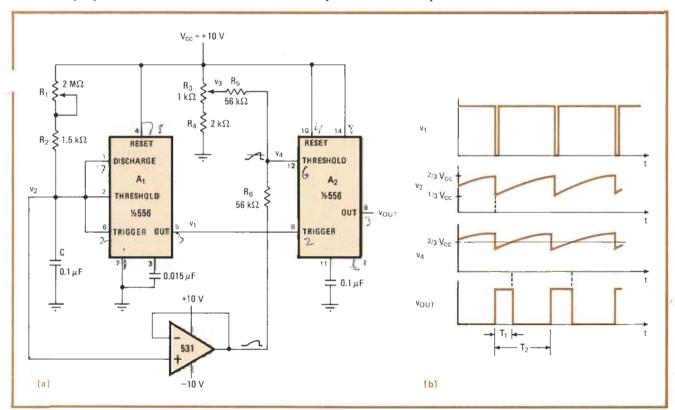
external resistance-capacitance elements, but by the voltage on the threshold port. The output of  $A_2$  will remain high if the threshold voltage stays below two thirds of the supply voltage,  $V_{\rm cc}$ . This circuit can generate a dc offset voltage at the port to modify the threshold-switching time.

The voltage at the threshold port is determined by the two input voltages,  $v_2$  and  $v_3$ , at the summing junction. Thus:

$$v_4 = v_2 \left( \frac{R_5}{R_5 + R_6} \right) + v_3 \left( \frac{R_6}{R_5 + R_6} \right)$$

Voltage  $v_2$  is an exponential ramp resulting from charging C through resistances  $R_1$  and  $R_2$ . The boundaries of the signal, determined by the internal comparators of  $A_1$ , lie between  $\frac{1}{3}$   $V_{cc}$  and  $\frac{2}{3}$   $V_{cc}$ .

The 531 op amp is a buffer for the high-impedance  $A_2$  signal and prevents current from flowing into the timing port, which could charge C from  $V_{cc}$  through  $R_5$  and  $R_6$ . Dc voltage  $v_3$  can be varied from  $^{2/3}$   $V_{cc}$  to  $V_{cc}$ . Thus it can be seen that  $R_3$  will determine how large a dc voltage is superimposed on  $v_2$ , thereby controlling the duty cycle. Since there are no feedback loops linking  $A_1$  and  $A_2$ , it is clear that frequency and duty cycle adjustments are independent.



**No relation.**  $A_1$  runs at frequency set by  $B_1$ . But duty cycle is selected by  $B_3$ , which controls signal offset at threshold port of  $A_2$ . No feedback loops link  $A_1$  and  $A_2$ , thereby ensuring independent adjustment of rep rate and duty cycle. Timing diagram details operation.